

Optical Data Interface Overview

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AXIe

Key Contributors:



- Chris Sutton
- Joe Mueller
- Lauri Viitas
- Ken Owens
- Marc Verdiell

- Chairman of AXle Consortium and sponsor:
Chris Miller, Keysight Technologies
- Chairman of AXle Technical Committee and facilitator:
Larry Desjardin, Modular Methods



Optical Data Interface – Why?

- Numerous measurement applications are now demanding higher data transfer speeds: 5G wireless, 100G and 400G wireline
- Very high speed data streaming challenges the limits of electrical interfaces, even for the fastest modular standards:

	Bus Speed (GB/sec)		
	PXIe: (PCIe x8)	AXIe: (PCIe x16)	AXIe Local Bus
PCIe Gen2	4	8	80 (demonstrated)
PCIe Gen3	8	16	

- Looking forward, significant interoperability issues arise for deploying PCIe Gen 4 in a backplane architecture
- Solution: adopt optical technology for >20GB/s data transfers



Optical Data Interface – What is it?

- Optical interconnect for very high speed streaming applications between instruments, processors, and storage
- 20GBytes/sec continuous streaming speed with a single optical cable
- Speed increases with multiple cables or optical bit rates
- Data streaming only (data plane). Commands are sent via the standard instrument and device interfaces.
- Data Format compatible with VITA 49, a Software Defined Radio packet structure.
- Works with instruments of any format: traditional boxes, PXI, or AXIe
- Managed by the AXIe Consortium as ODI family of specifications
- Abbreviated as ODI



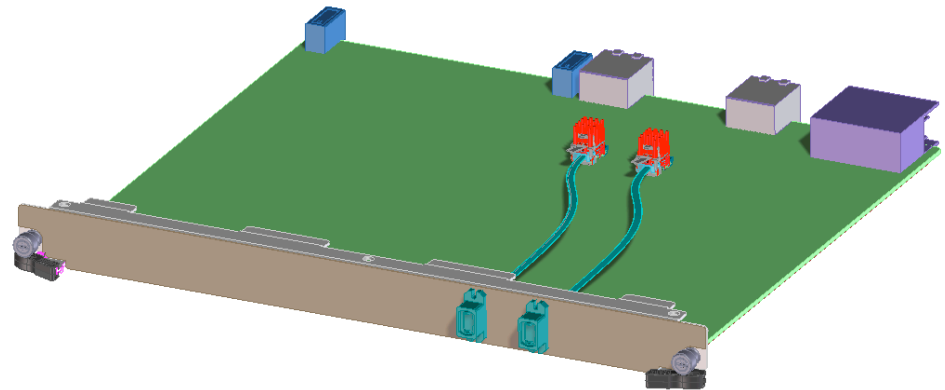
ODI works with any device format

- ODI defines a standardized optical connector and optics, known as an optical port.
- ODI ports may be placed on any PXI, AXIe, LXI, or USB instrument.
- ODI ports may be placed on any processor, storage device, or plug-in card.
- All data transfer and flow control occurs over the pluggable optical cable. There is no need for any additional cables, optical or electric.

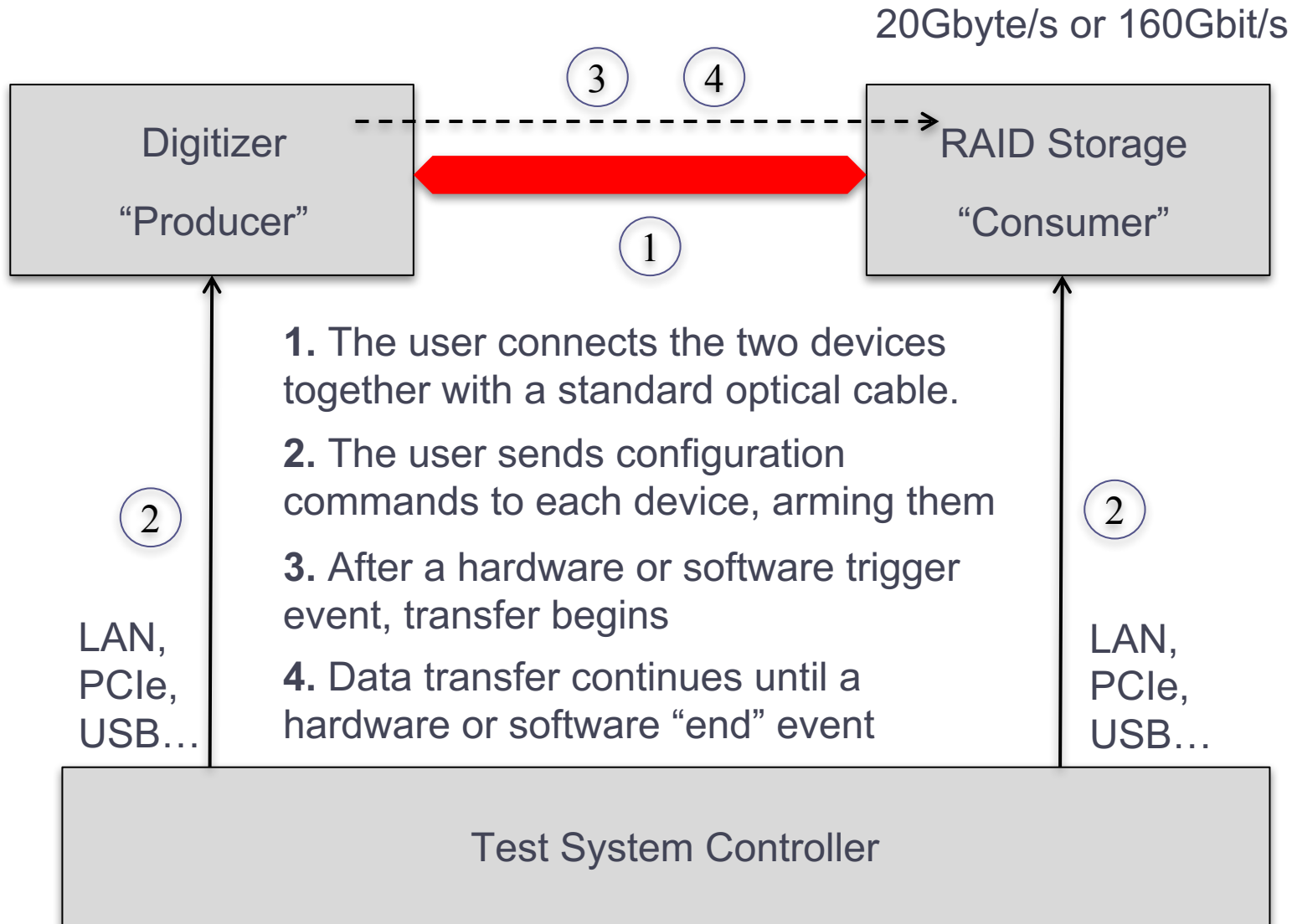
Example: PCIe plug-in board with memory and FPGA processing, supporting two optical ports on faceplate



Example: AXIe module with two faceplate optical ports

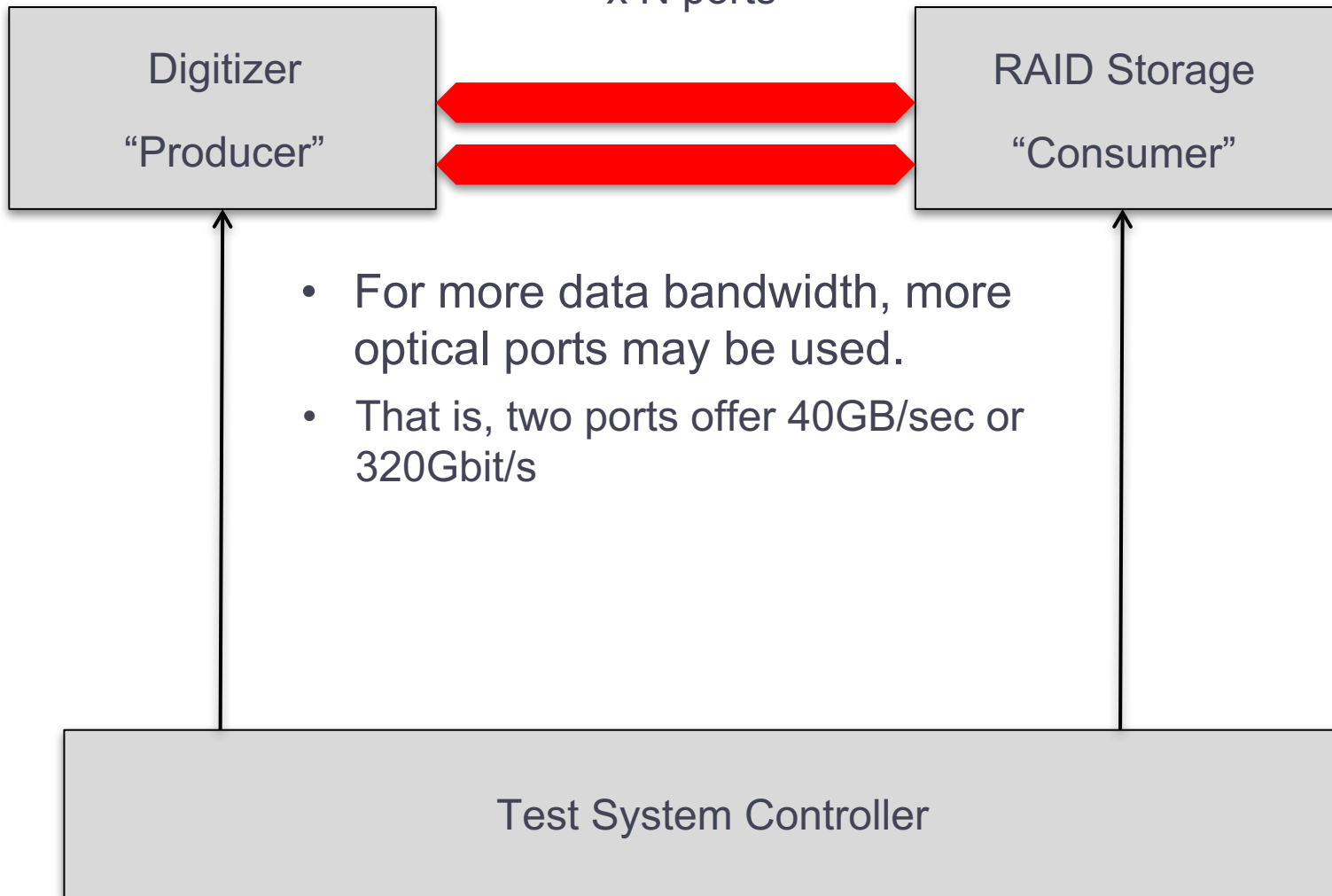


Example operation: Storage

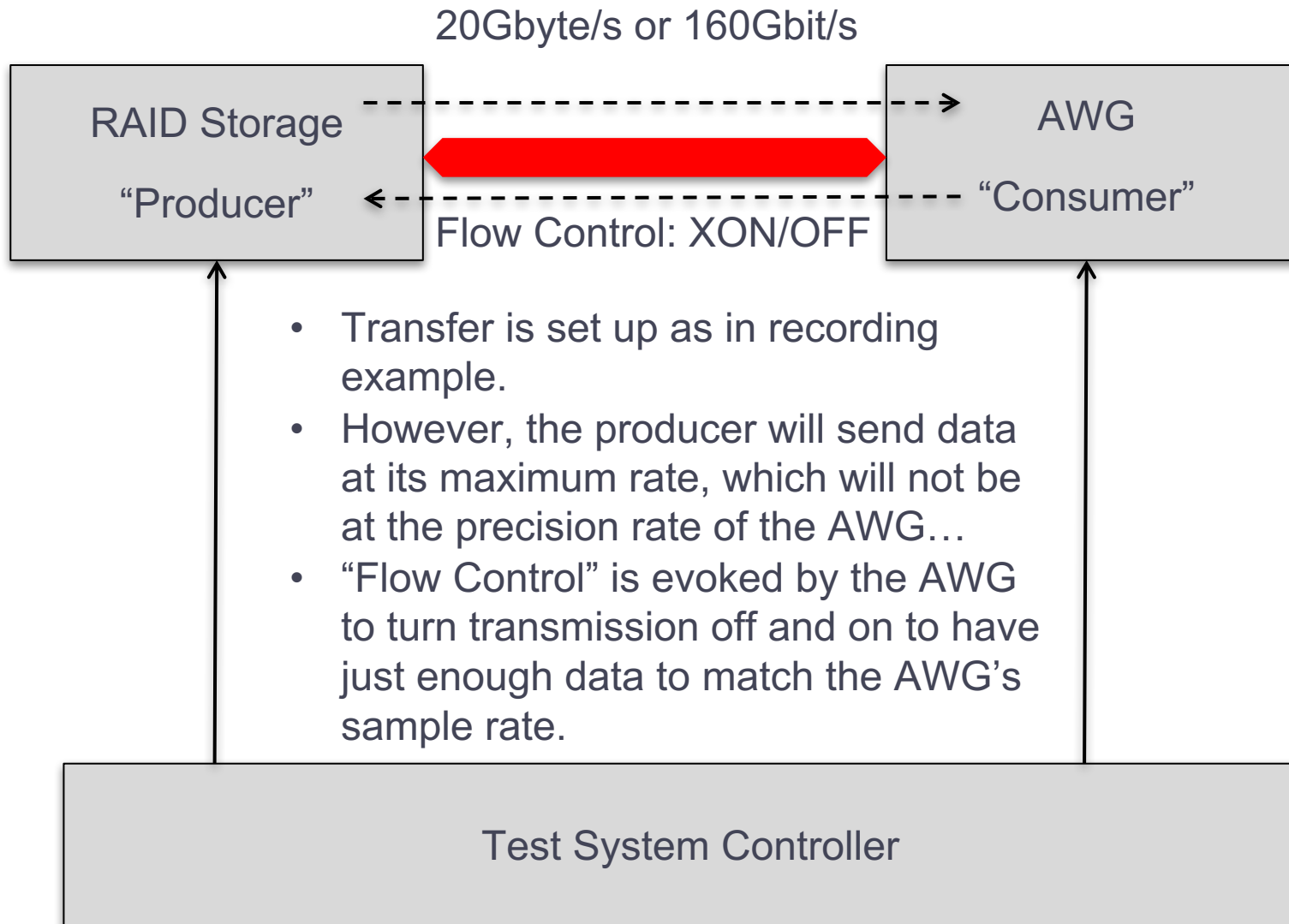


Port aggregation increases data throughput

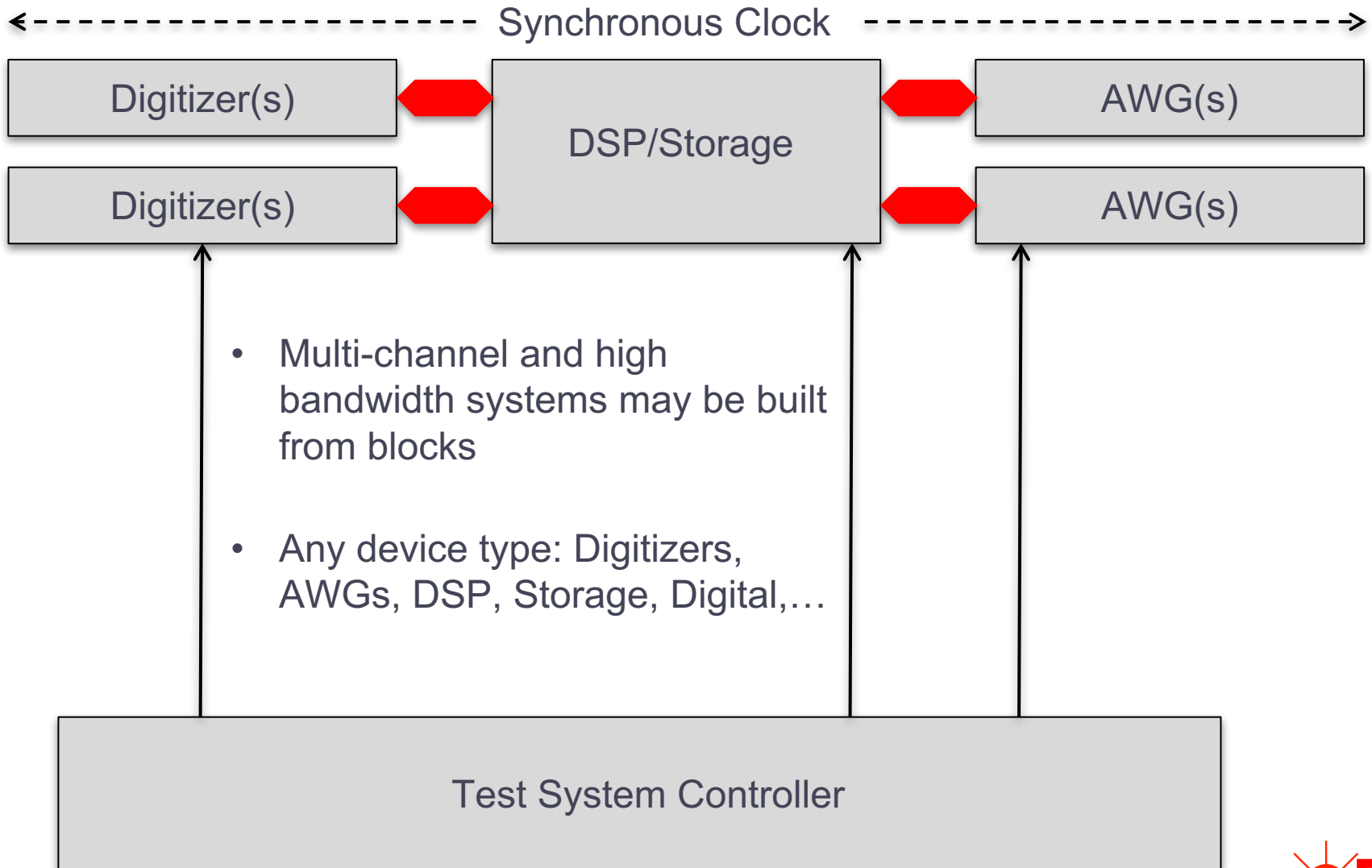
(20Gbyte/s or 160Gbit/s)
x N ports



Playback of recorded or computed data



Systems may be built from blocks:



T&M Markets

Physics - Science Industrial Automotive Aerospace & Defense Wireless Comms Wireline Comms Digital & Semi Consumer Other



Embedded



R&D



Manufacturing



Maintenance



Monitoring





ODI Markets

Physics-Science Industrial Automotive Aerospace & Defense Wireless Comms Wireline Comms Digital & Semi Consumer Other



Big Physics

Embedded



Avionics/SDR

Receiver Test

R&D



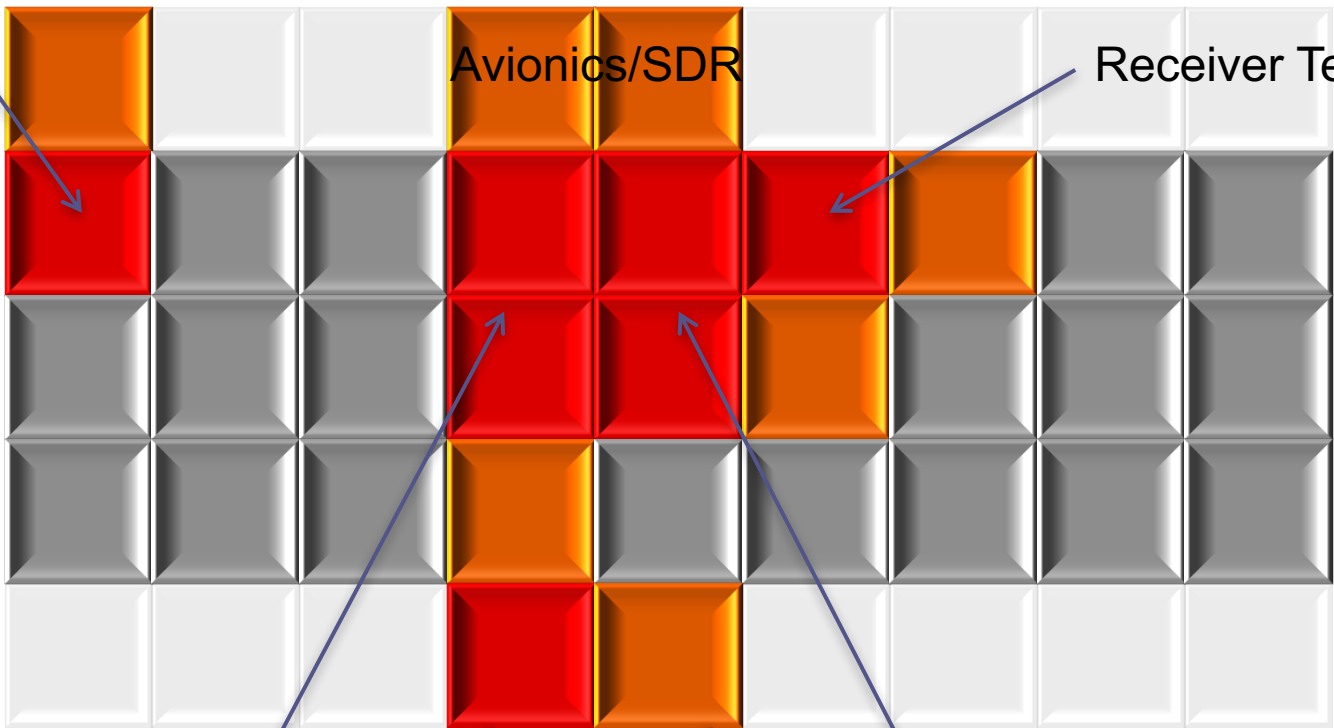
Manufacturing



Maintenance



Monitoring



Phased array radar/EW

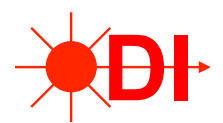
Spectral Monitoring

5G

Traditional T&M market

ODI Markets

ODI Upside



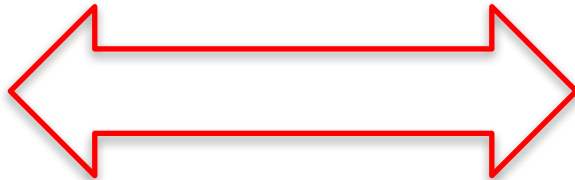
Three fundamental layers – all leveraged

VITA 49 “VRT” Data Packets



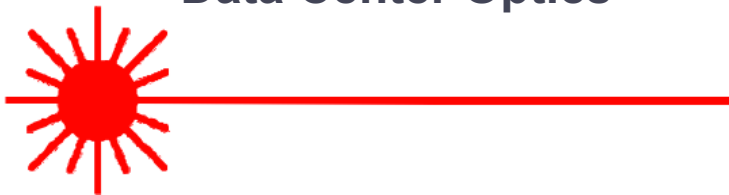
- VITA Radio Transport
- Standard data formats
- Multiple channels
- Storage framing
- SDR compatible

Interlaken Interconnect Protocol



- Packet Framing
- Flow Control
- SerDes Management
- FPGA independent

Data Center Optics



- 850nm VCSEL
- Multimode fiber
- 12 Tx & 12 Rx lanes
- 12.5Gb/s & 14.1 Gb/s



ODI 3-part Specification

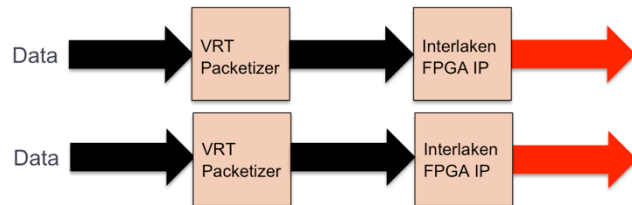
ODI-2.1: High-Speed Formats

- 8 to 16 bit data formats
- Packing Methods
- Optimized for SDR & 5G

Data
Formats



ODI-2: Transport Layer



- VITA-49 “VRT” Packets
- FPGA Optimized
- Port Aggregation
- Context Packets

Transport
Layer

ODI-1: Physical Layer



- 12 lane multimode optics
- 12.5 & 14.1 Gb/s
- Interlaken Protocol
- Flow Control

Physical
Layer



Optical Layer portion of Physical Layer

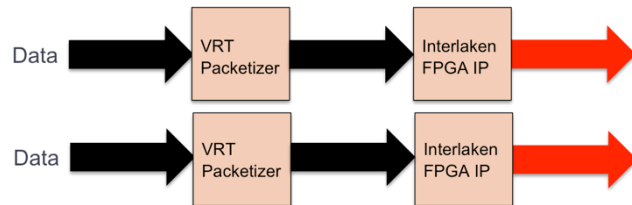
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ODI-1: Physical Layer

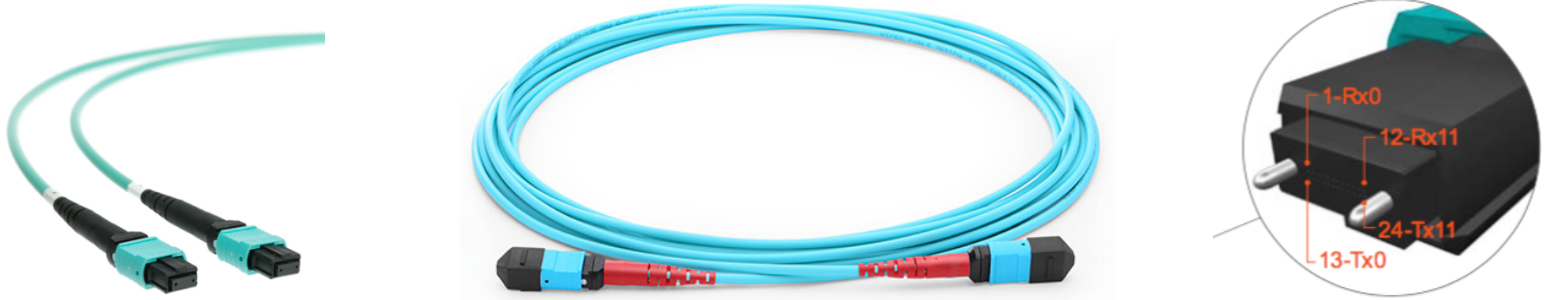


- 12 lane multimode optics
- 12.5 & 14.1 Gb/s
- Interlaken Protocol
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Physical
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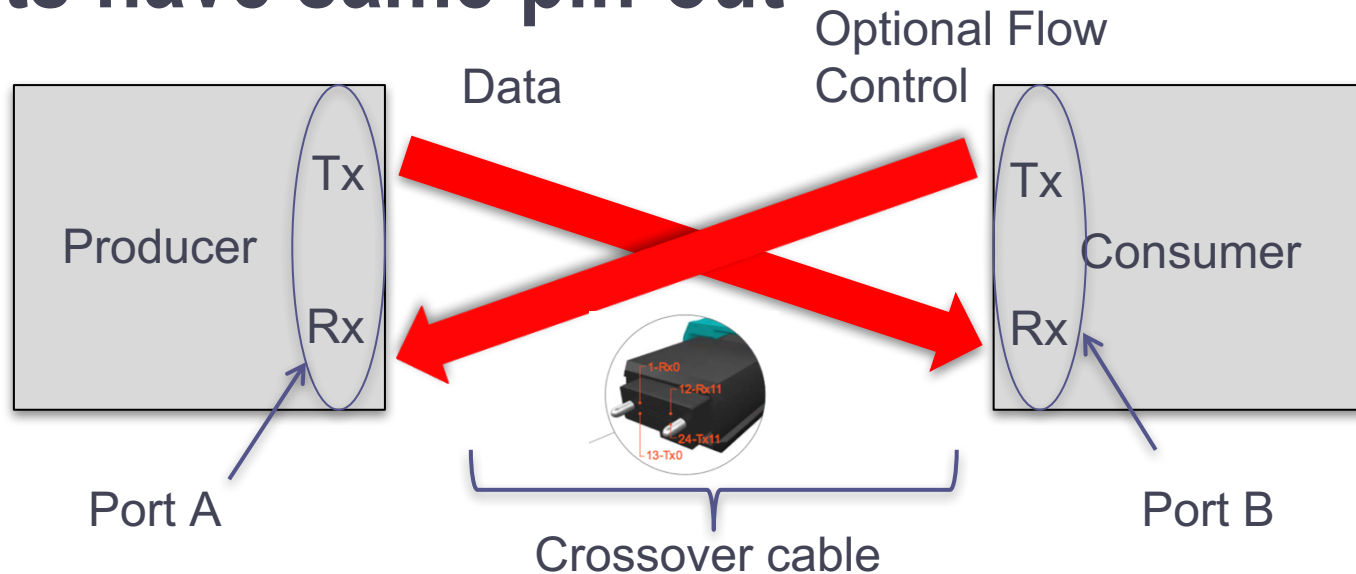
Optical Cable



- A single bi-directional multiple fiber cable for all optical links
- 24 lanes: 12 lanes in each direction, crossover configuration
- OM3 850nm multimode fiber with MPO/MTP female connectors
- 14.1Gb/s on each lane enables 20GB/s in each direction
- 12.5Gb/s rate for economy applications on same fiber
- Non-directional: Either end may be plugged into any device
- Cable is capable of higher speeds as optical Tx/Rx rates increase
- Up to 100 meters in length



All ports have same pin-out



- Standard Port has Tx and Rx in same position, regardless if Producer or Consumer
- Standard cable is 12 fibers each direction, in crossover configuration.
- A port is allowed to implement either 12 lanes in either directions, or zero.
- A digitizer may have uni-directional port, while an AWG may have a bi-directional port for flow control



Optics

- 850nm multimode transmitters and receivers
- Class 1 laser product, meaning no safety issues during normal use
- 802.3ba optical levels, 12.5Gb/s or 14.1Gb/s on each lane
- 12 VCSEL transmitters
- Can be implemented with Samtec Firefly components

CLASS 1 LASER PRODUCT



FIREFLY™

Micro Flyover System

Patented

The FireFly™ Micro Flyover System is the first interconnect system that gives the designer a choice of using either micro footprint optical or copper interconnects to meet today's data rate requirements and the next generation.

The FireFly™ system enables chip-to-chip, board-to-board, on-board and system-to-system connectivity at data rates up to 28 Gbps. FireFly™ is based on a high performance interconnect system which allows the use of low-cost copper cables or high performance active optical engines.





Protocol Layer portion of Physical Layer

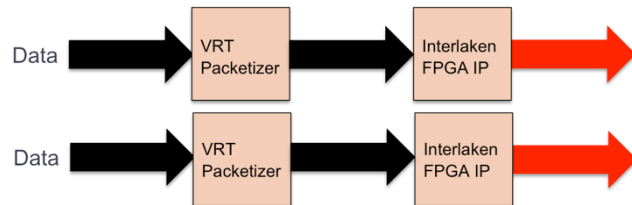
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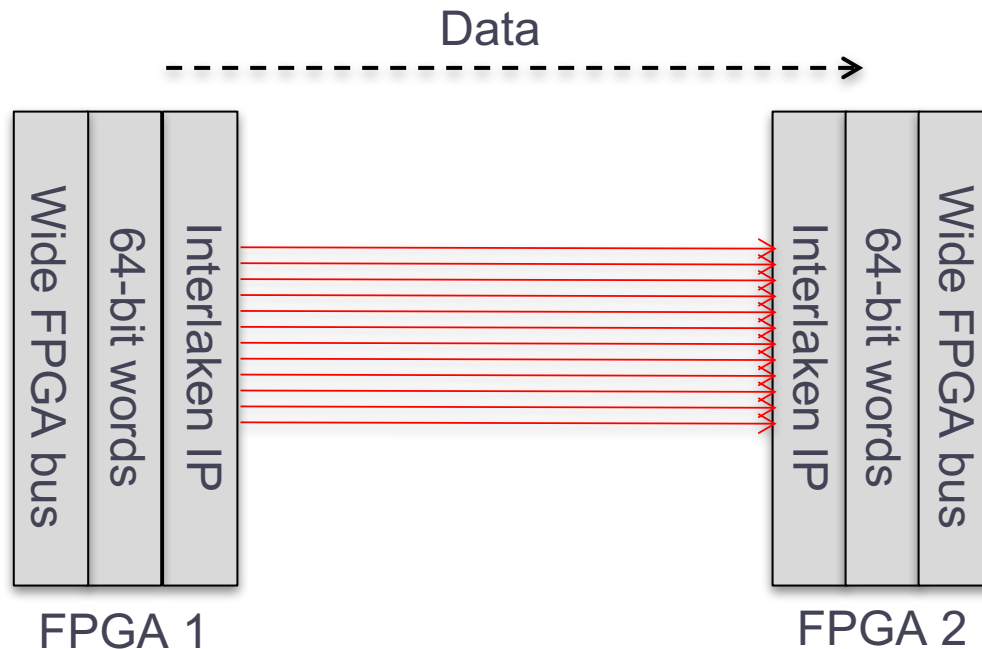
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Physical
Layer

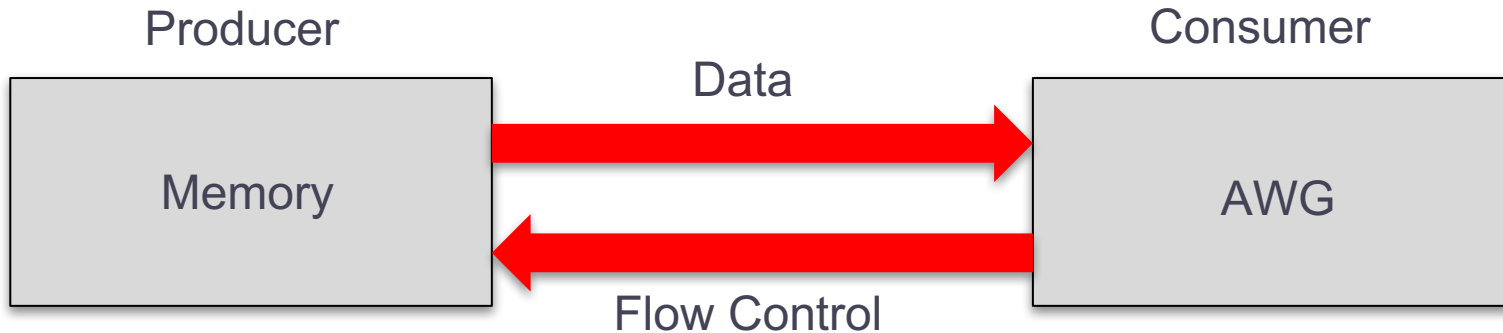


What is Interlaken?

- A chip-to-chip protocol developed by Cortina Systems and Cisco Systems
- Allows wide data patterns typically on FPGAs to be sent over any number of serial links and speed
- Based on 64-bit words, works well with wide FPGA buses
- Includes optional flow control



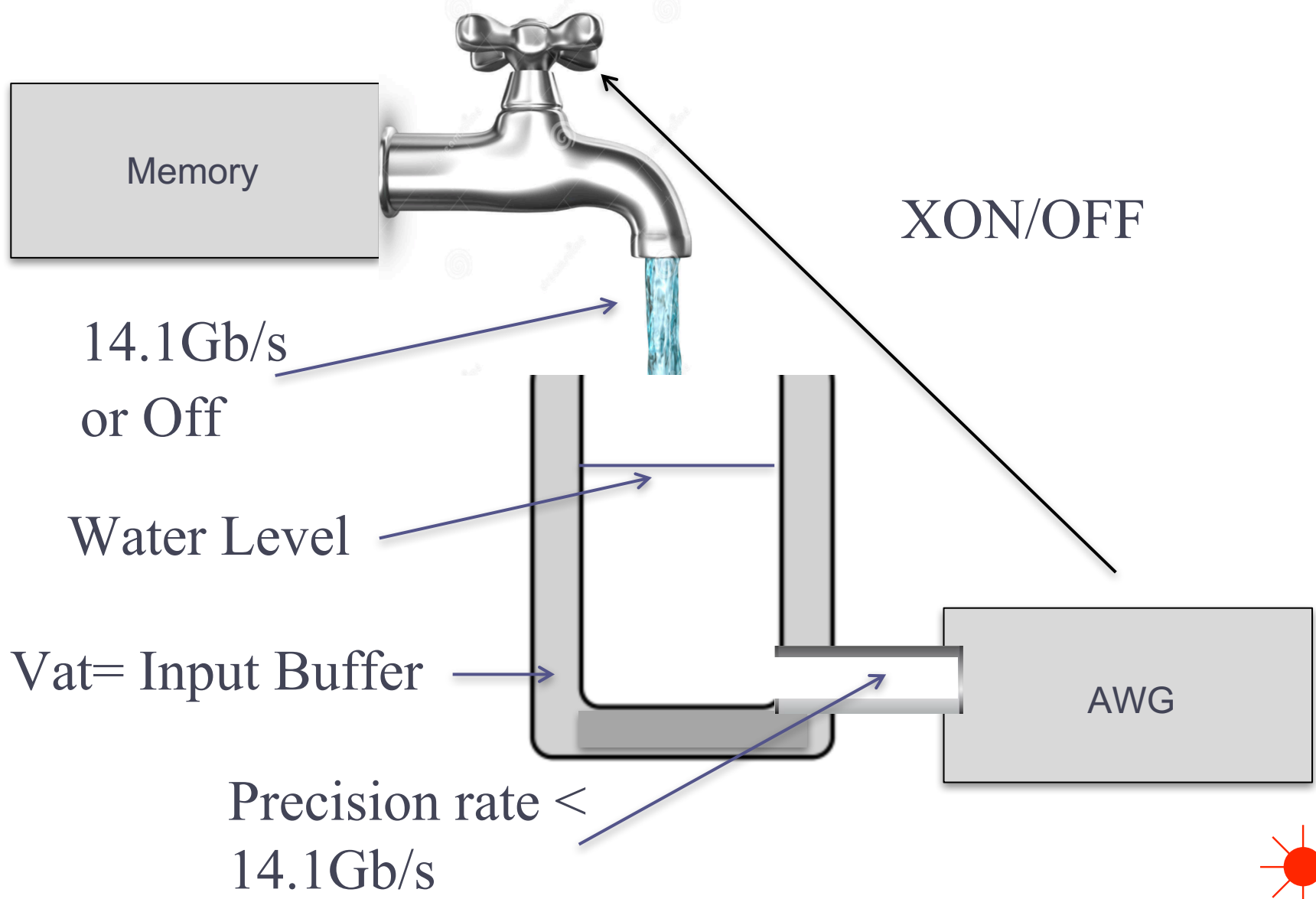
Interlaken chosen as the interconnect protocol



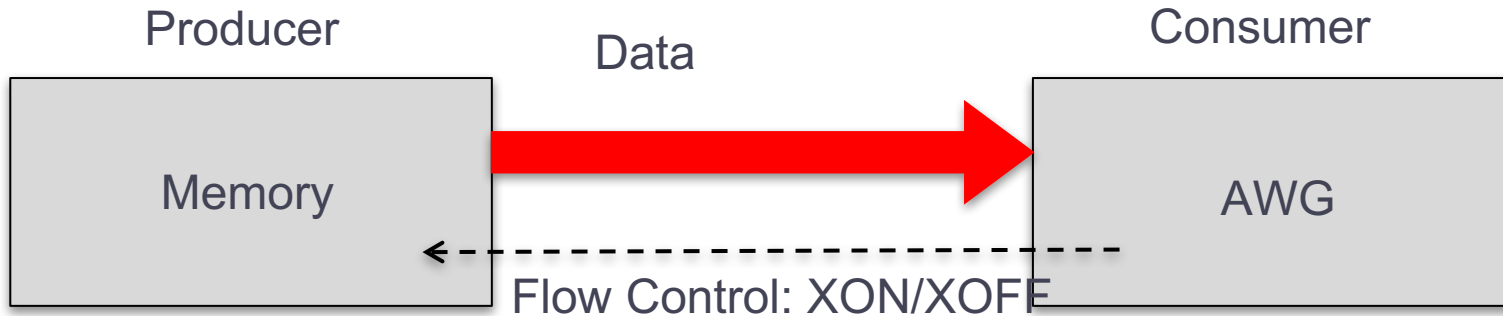
- A proven protocol for high speed chip to chip transfers
- Efficiently packs data over a number of lanes, in this case 12 lanes.
- FPGA vendor-independent
- In-band flow control avoids additional cables between devices
- Out-of-band flow control allows a cost-effective alternative
- Only a single Interlaken channel is typically used.
- Supports long bursts for minimum overhead.
- Supports the transfer of packets, which enables multi-port synchronization



Flow Control – Analogy to a water tank



Flow Control



- **Optional** flow control allows a consumer to modulate the rate of the data being sent to it by sending a signal **XON/XOFF** (Transmit ON, Transmit OFF) to the producer.
- The flow control signal XON/XOFF may either be sent “**In Band**” (IB) or “**Out of Band**” (OOB). That is, it may be sent via a **reverse Interlaken link**, or as a **separate electrical or optical signal**.
- **Consumers such as AWGs** and other signal generators are likely to implement flow control to keep the incoming data patterns matched with their sampling speed
- **Producers such as digitizers** are more likely to **not** implement flow control, since they must generate data at their sampling speed.
- **Memory, other storage devices**, and processors are likely to implement **both**, flow control and no flow control, to interface with all instrument types.



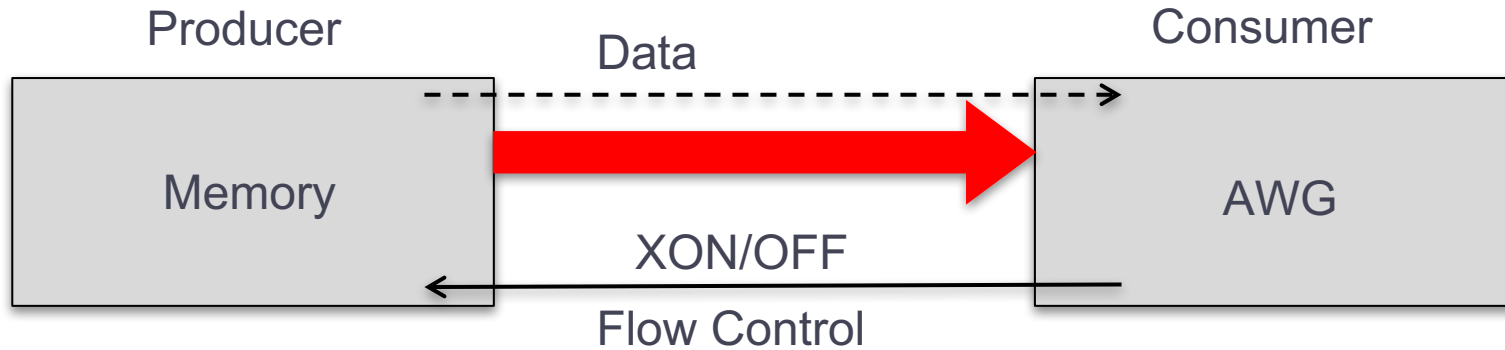
Flow Control – In Band



- In band flow control is implemented over the optical cable by the consuming device sending Interlaken XON and XOFF commands (shown above) over the optical reverse path.
- XON causes the producer to send data at its full rate.
- When a consumer detects that its input buffers are getting close to full, it then sends XOFF, forcing the producer to stop transmitting after it has completed the current Interlaken burst.
- When the consumer detects that the buffer is sufficiently depleted, but before it is empty, it sends the XON command to the producer to resume transmitting.
- This protocol allows the consumer to pace the data being sent to it.



Flow Control – Out of Band



- Out of band flow control operates identically to In Band, except that the XON/XOFF signal is sent over an electrical or optical wire.
- Electrical flow control allows unidirectional optical ports to implement flow control without the cost of a reverse optical link.
- Recommendation: A device that implements flow control SHOULD have an external electrical connector that implements XON/XOFF for each optical port.
- Recommendation: AXIe and PXI modular devices SHOULD implement electrical flow control using the backplane trigger lines, one line per port controlled. If implemented, each flow control signal MUST be programmable to use any of the backplane trigger lines.
- When using an electrical connection, 1=XON, and 0=XOFF



Interlaken Protocols: BurstMax

- Interlaken sends data through a series of data bursts. In most cases, the length of the data burst is a parameter labeled BurstMax
- Longer BurstMax is more efficient. 256 BurstMax is often free.
- ODI specifies two BurstMax options.
 - 256 bytes at 12.5Gb/s line rate for economy applications
 - 2048 bytes at 14.1Gb/s for performance applications
- All 12.5Gb/s producers must transfer data using 256 byte BurstMax
- All 14.1Gb/s producers **MUST** transfer data using 2048 byte BurstMax
- Higher speed devices (e.g. 14.1Gb/s) **MUST** operate at lower speeds unless the device is unusable at the lower speed



Speed Calculation – long BurstMax

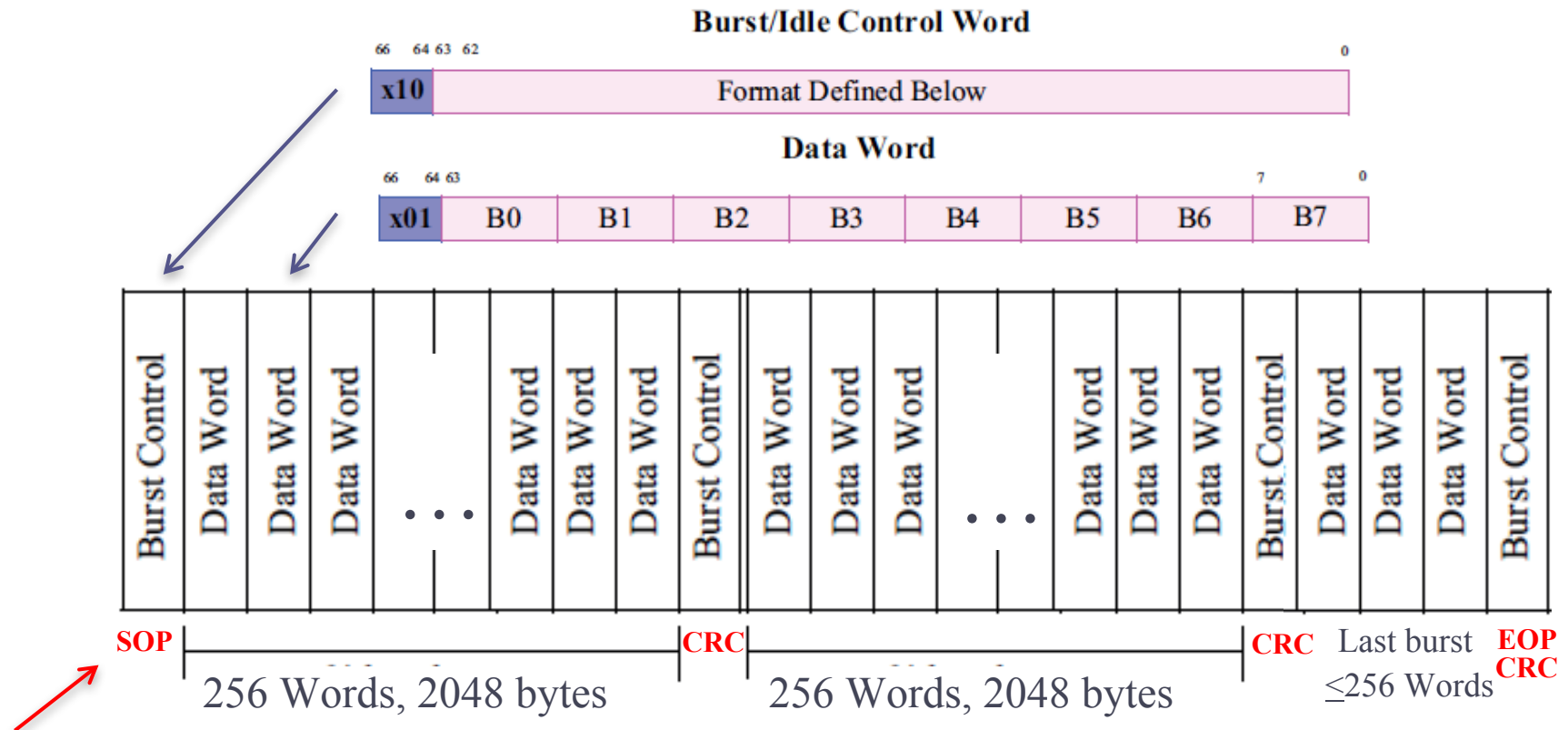
- $14.1 \text{ Gb/s} \times 12 \text{ lanes} / 8 \text{ bits/byte} \Rightarrow 21.15 \text{ GB/sec}$ raw channel speed
- $64/67 \text{ coding} = 95.52\% \text{ efficiency} \Rightarrow 20.20 \text{ GB/sec}$ coded speed
- $256 \text{ word (2K byte) burst framing} = 256 \text{ words}/257 \text{ words}$
= 99.61% efficiency
 $\Rightarrow 20.12 \text{ GB/sec}$ framed speed
- Alignment efficiency = 100%. $\Rightarrow 20.12 \text{ GB/sec}$ aligned frame speed
- $2048 \text{ Metaframing} = 2044 \text{ words}/2048 \text{ words} = 99.8\% \text{ efficiency}$
 $\Rightarrow 20.09 \text{ GB/sec}$ total speed



Interlaken framing choices - long

Burst framing, set at 256 words = 2048 bytes

Burst framing sends the data in 2K byte chunks



Start of Packet and End of Packet encapsulate one VRT packet.



Transport Layer: Introduction of Packets

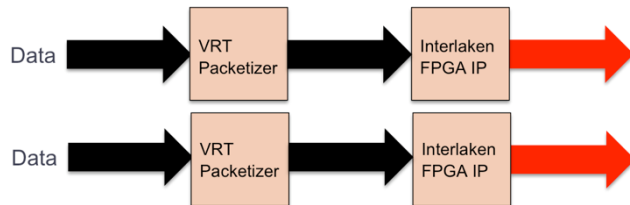
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- 8 to 16 bit data formats
- Packing Methods
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Data
Formats

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ODI-2: Transport Layer



- VITA-49 “VRT” Packets
- FPGA Optimized
- Port Aggregation
- Context Packets

← Transport
Layer

ODI-1: Physical Layer



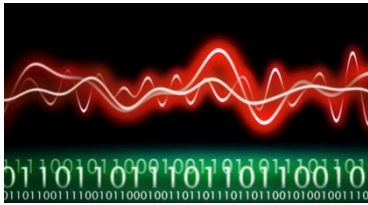
- 12 lane multimode optics
- 12.5 & 14.1 Gb/s
- Interlaken Protocol
- Flow Control

Physical
Layer



Packets are fundamental to ODI

VITA 49 “VRT” Data Packets

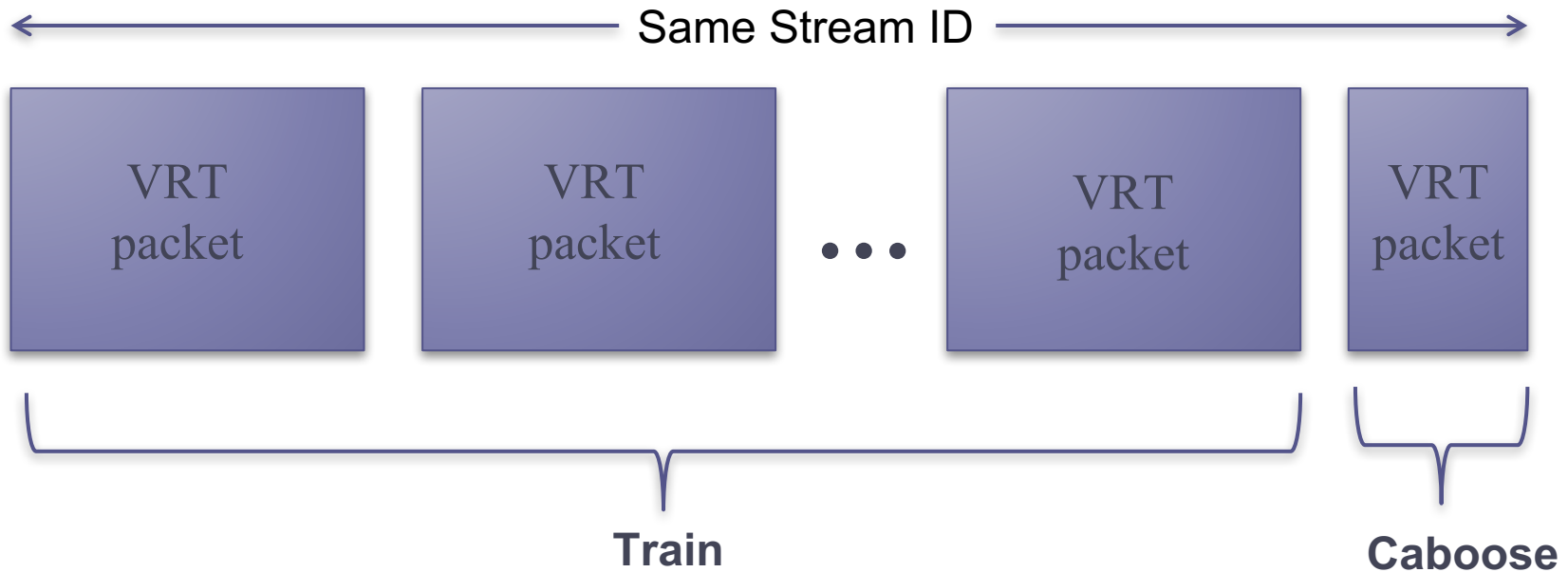


- VITA Radio Transport
- Standard data formats
- Multiple channels
- Storage framing
- SDR compatible

- Packets are bracketed by Interlaken SOP and EOP signals
- Packets contain single channel or multi-channel sample data
- Packet boundaries allow for error recovery
- Packets allow port aggregation and synchronization
- Consecutive packets are sent to stream data
- All data is stored as packets
- Packets are independent of the underlying transmission method
- Packets are compliant with VITA 49 standard



Streaming via consecutive packets



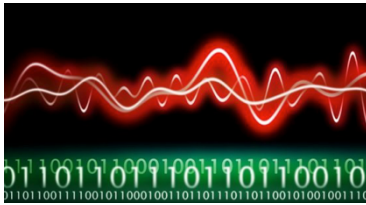
Streaming is performed by transmitting a series of large VRT packets consecutively in a “train”. These packets are designed for efficiency, and typically are of the same size and number of samples. They are chosen to contain integer number of Interlaken words, and have good properties with the FPGA’s internal bus width.

When streaming ends, the final packet is called the caboose. It may be the same size as the previous packets, or it could be smaller.

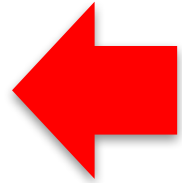


What is VITA 49?

VITA 49 “VRT” Data Packets



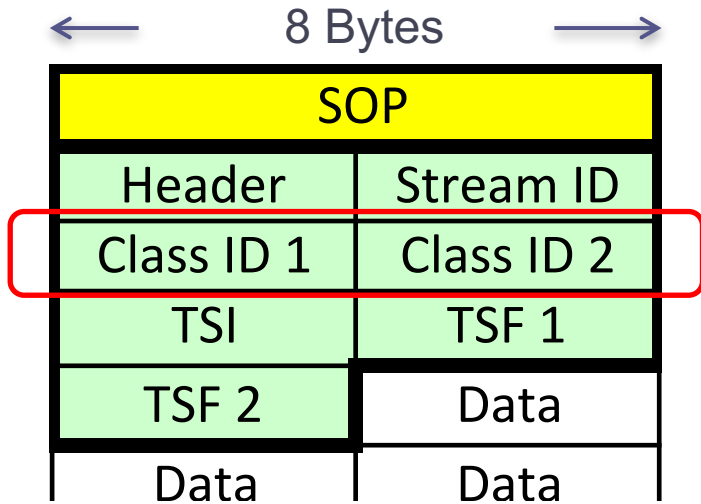
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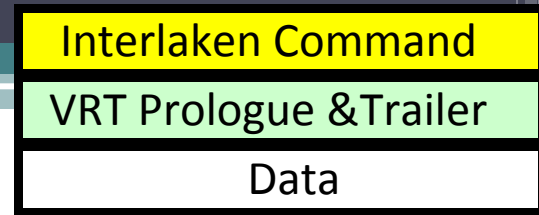
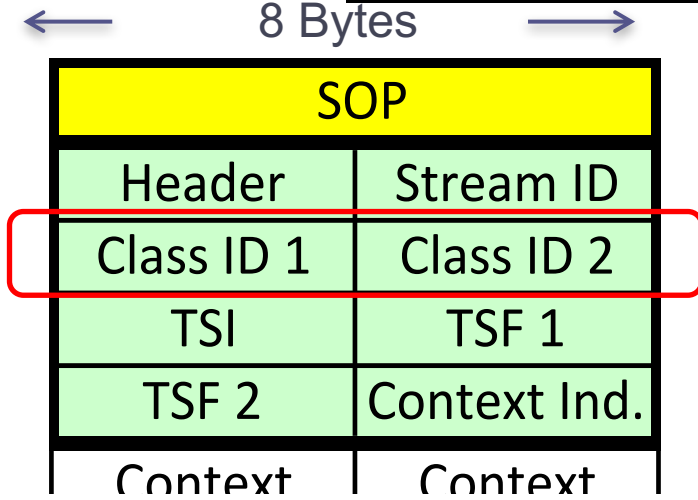
- VITA 49 = VITA Radio Transport standard a.k.a VRT
- Family of specifications for transferring data within a radio
- Defines packet structure, data formats, and context info
- Deployed by software defined radio vendors for mil/aero
- Actual standard not specific to radios or communications
- ODI-2 defines a standard method of sending arbitrary block data and flexible context packets consistent with the VRT specification. ODI-2 adds constraints, such as 32-byte boundaries, to optimize its use with FPGAs.
- ODI defines a VRT-compliant subset for optimally sending multi-channel 8 to 16 bit data streams, called ODI-2.1
- ODI could be adopted by mil/aero community for embedded. It is not restricted to test and measurement



VRT Classes



Class ID
Fields



Data Packets

Context Packets

- VITA 49 includes the concept of classes. Classes define the parameters of the data that follows, such as data type, data format, data packing, etc.
- The Class ID fields, sent in the Prologue before the actual signal or context data, uniquely define the parameters of the data that follows.
- The AXIe Consortium, using its OUI (Organizationally Unique Identifier) has defined a number of classes oriented towards the transfer of high-speed data.
- The slides that follow show packets that comply with the ODI packet classes, and do not necessarily describe general VRT packets.



Packet structure - Data

← 8 Bytes → = 1 Interlaken Word

SOP	
Header	Stream ID
Class ID 1	Class ID 2
TSI	TSF 1
TSF 2	Data
Data	Data
Data	Data
Data	Data
Data	Data
Data	Data
Data	Data
Data	Data
Data	Data
Data	Trailer
EOP	

← Interlaken Start of Packet Command

VRT Data Prologue. 28 Bytes.

Stream ID, Length of packet, Data formats,
Optional time stamps

Data Payload

Up to 256 Kbytes of data

Always a multiple of 32 bytes

Typically long (>16K) to get efficiency

← VRT Trailer (errors, overload, events)

← Interlaken End of Packet



Interlaken Command

VRT Prologue & Trailer

Data

Packet structure - Context

← 8 Bytes → = 1 Interlaken Word

SOP	
Header	Stream ID
Class ID 1	Class ID 2
TSI	TSF 1
TSF 2	Context Ind.
Context	Context
Context	Context
Context	Context
Context	Context
Context	Context/Pad
Context/Pad	Context/Pad
Context/Pad	Context/Pad
Context/Pad	Context/Pad
EOP	

← Interlaken Start of Packet Command

VRT Context Prologue. 32 Bytes.

Same as VRT Data Prologue plus Context Indicator field

Context Fields

Always a multiple of 32 bytes

Final 32 bytes will include final context fields, plus any "Pad" bytes of null data to insure context packets are always a multiple of 32 bytes.

← Interlaken End of Packet



Scalable Speed

Today

		Link Speed			
		ODI-1.0		ODI-1.1	ODI-1.2
		12.5G	14.1G	28G	56G
# of Ports	1	17.3GB/s	20GB/s	40GB/s	80GB/s
	2	34.6GB/s	40GB/s	80GB/s	160GB/s
	3	51.9GB/s	60GB/s	120GB/s	240GB/s
	4	69.3GB/s	80GB/s	160GB/s	320GB/s



- Data transfer speeds may be increased by increasing the link speed or by using additional ports.
- ODI-2.0 specifies how ports are aggregated to achieve higher speeds
- A higher speed device **MUST** operate at lower speeds, unless it becomes unusable
- Ports **MAY** be bound together for higher speeds.
- There is no requirement that a device that has multiple ports must support binding. The multiple ports may be available for separate data streams, such as a combination producer and consumer



Scalable Speed

Planned

		Link Speed			
		ODI-1.0		ODI-1.1	ODI-1.2
		12.5G	14.1G	28G	56G
# of Ports	1	17.3GB/s	20GB/s	40GB/s	80GB/s
	2	34.6GB/s	40GB/s	80GB/s	160GB/s
	3	51.9GB/s	60GB/s	120GB/s	240GB/s
	4	69.3GB/s	80GB/s	160GB/s	320GB/s

- Each generation may not exactly double in speed.
- All 28Gb/s devices must support the ODI-1.0 12.5Gb/s and 14.1Gb/s speeds.
- 28Gb/s devices will likely be narrowband optical devices. That is, they will have a small range of allowable bit rate at approximately 28Gb/s. However, they will still be able to operate at 12.5Gb/s and 14.1Gb/s.
- 56Gb/s devices are too preliminary to know their backwards compatibility. An alternative to doubling the bit rate would be to double the lanes to 24.



Aggregating Ports

Multiple optical ports may be synchronized to increase data throughput.

Ports are aggregated by synchronizing the VRT packets across multiple ports. There are two use cases to aggregating ports:

- **Multi-channel data**
 - In this case, a subset of channels is streamed from each port within the VRT stream of that port, and sent simultaneously. All VRT signal data packets have the same sample length. That is, if Port A has 8K samples of each of its channels, Port B will have 8K samples for each of its channels.
- **Single-channel data**
 - A data stream from a single channel may be divided into two or more VRT streams, with consecutive samples directed to alternating ports in a round robin fashion. All VRT signal data packets have the same packet length.



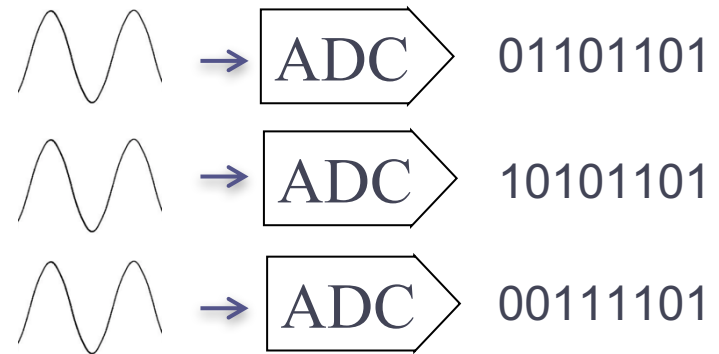
Ports and Channels - Definition

- Ports
 - Ports are separate optical connections, each at the end of an optical link.



Example of a two-port device

- Channels
 - Channels refer to separate electrical signals measured or generated by a device, or their digital representation.

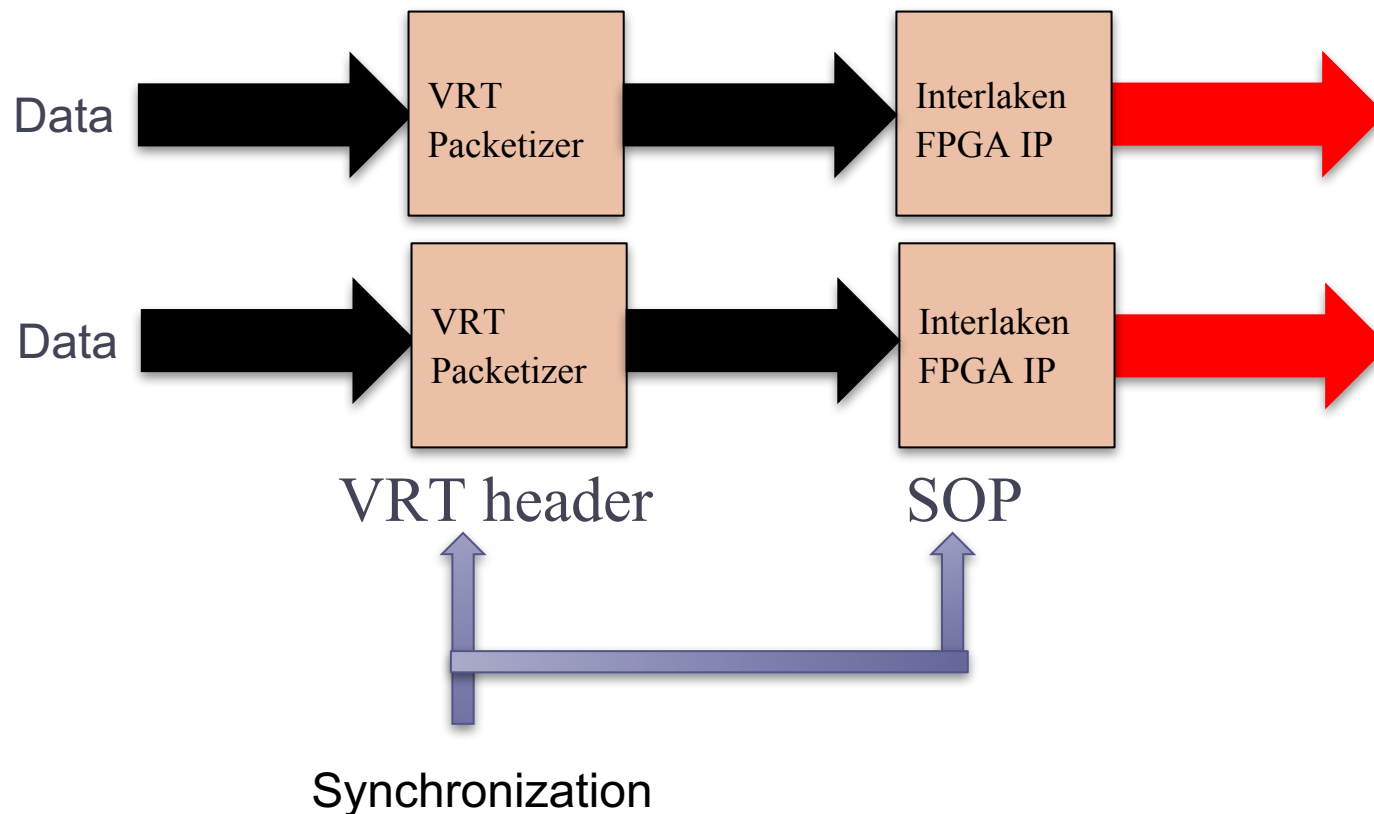


Example of 3-channel signal acquisition



Aggregating Ports – Synchronizing Packets

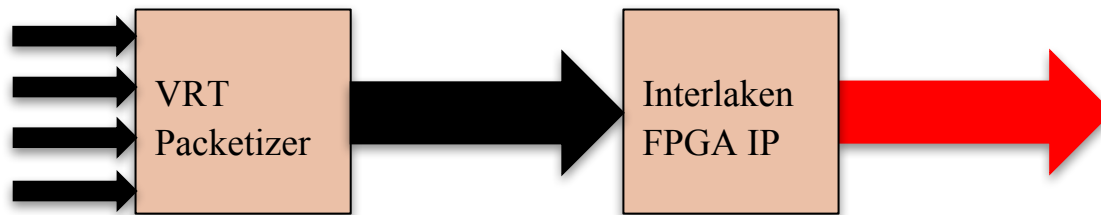
Synchronization occurs by sending equal-sample-length VRT packets simultaneously. The beginning of all packets will start at the same time, indicated by an Interlaken SOP signal. EOP may not occur on all ports simultaneously, but often does. The VRT packetizer consists of inserting 28 leading bytes and 4 trailing bytes around the block data, as defined by VRT.



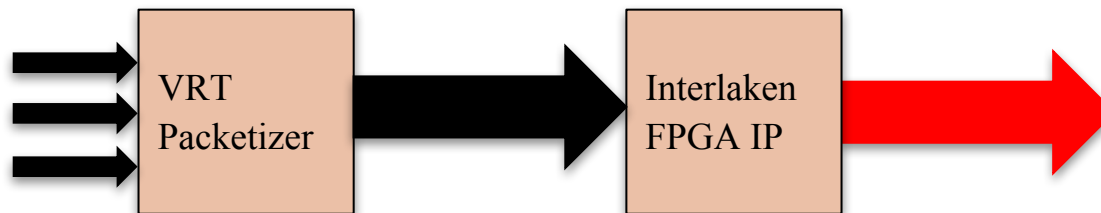
Aggregating Ports – Multiple channels

Synchronization occurs by sending equal-sample-length VRT packets simultaneously. The beginning of all packets will start at the same time, indicated by an Interlaken SOP signal. EOP may not occur simultaneously, but must occur before the next SOP.

Channels A,B,C,D



Channels E,F,G

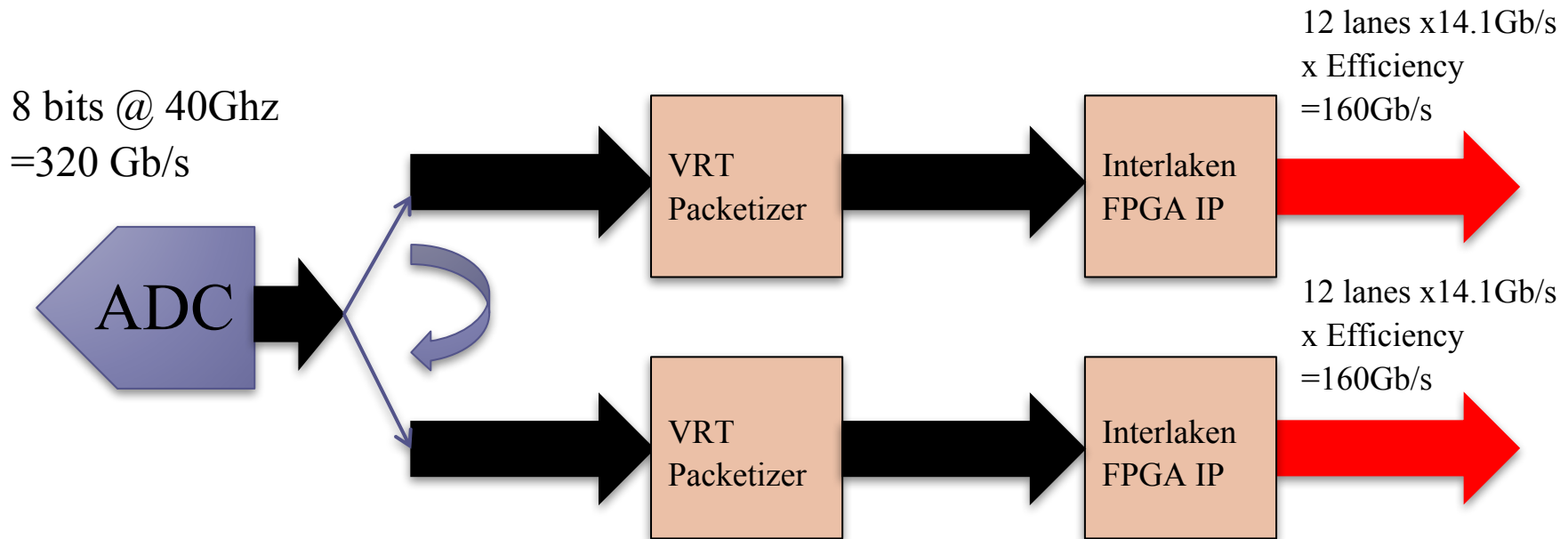


In the example above, all packets include the same number of samples per channel. Therefore, the packet size of Port 1 will be 1.33x that of Port 2.



Aggregating Ports, 1 channel– Transmission

Samples of a single channel are sent in a round robin fashion to each port, packaged in a VRT packet.



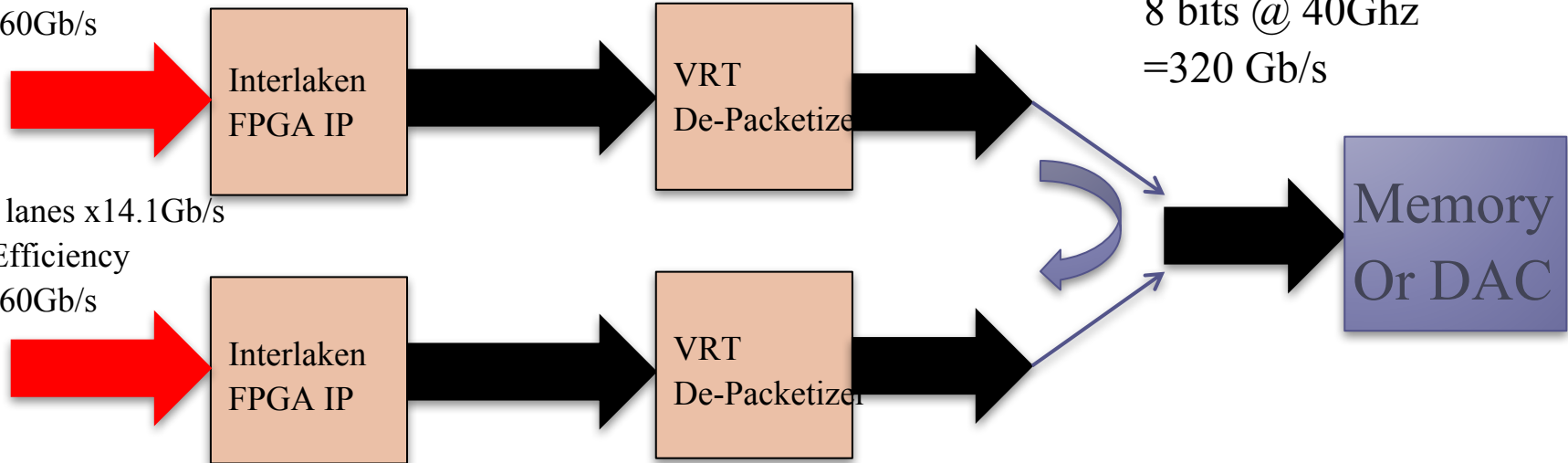
- Consecutive samples are transmitted in a round robin technique to each port.
- Interlaken SOP bit set on each port at beginning of VRT packet. This allows port alignment.
- The example shows 2 port aggregation. Any number of ports may be aggregated.



Aggregating Ports, 1 channel – Reception

VRT Packets are extracted from each port, and the data interleaved again to form the original stream.

12 lanes x 14.1 Gb/s
x Efficiency
= 160 Gb/s



12 lanes x 14.1 Gb/s
x Efficiency
= 160 Gb/s

8 bits @ 40 GHz
= 320 Gb/s

- Interleaved data in a round robin technique to create original stream
- Interlaken SOP bit set on each port at beginning of VRT packet. This allows port alignment.
- The example shows 2 port aggregation. Any number of ports may be aggregated



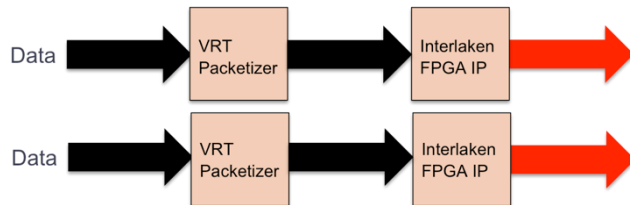
ODI-2.1: Standard High-Speed Data Formats

ODI-2.1: High-Speed Formats

- 8 to 16 bit data formats
- Packing Methods
- Optimized for SDR & 5G



ODI-2: Transport Layer



- VITA-49 “VRT” Packets
- FPGA Optimized
- Port Aggregation
- Context Packets

Transport Layer

ODI-1: Physical Layer



- 12 lane multimode optics
- 12.5 & 14.1 Gb/s
- Interlaken Protocol
- Flow Control

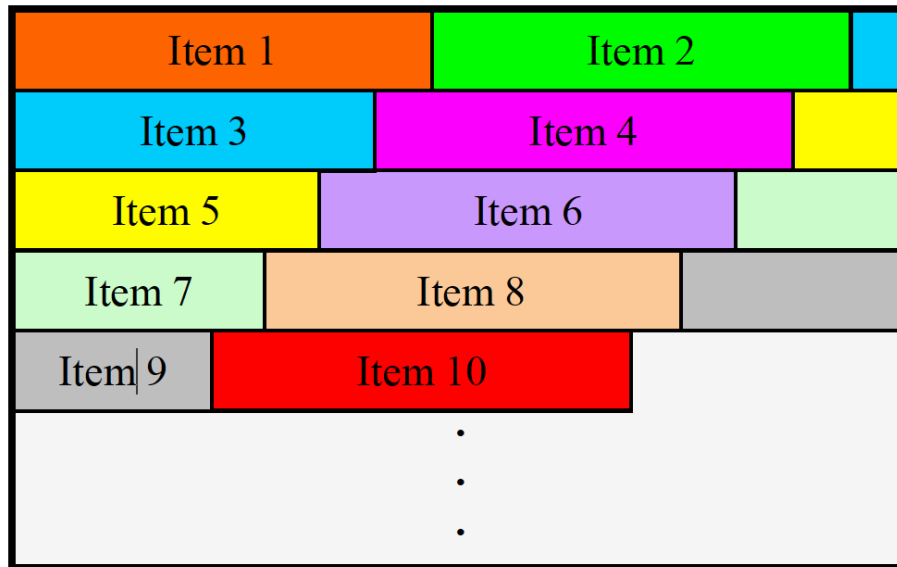
Physical Layer



Data Payload- two packing methods

Link efficient: packed most efficiently, word boundaries ignored

Processing efficient: Always start on 32 bit boundaries



Link-efficient packing



Processing-efficient packing

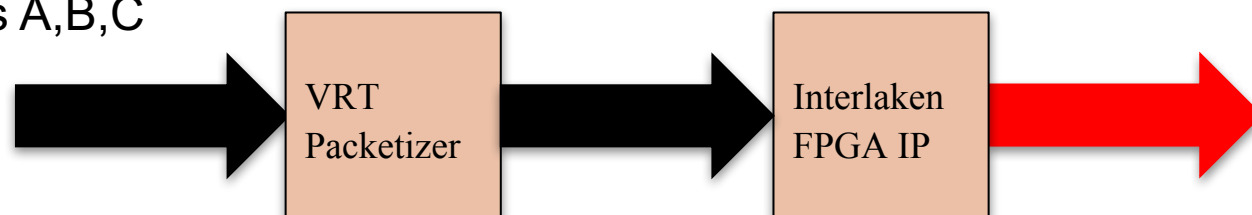
The above image is Figure 6.1.6.2-1 from the VITA 49.0 specification. It shows how 15-bit data is packed using link-efficient and processing-efficient packing respectively.



Multi-channel Data

- Data is sent in a round robin manner from each channel
- Each sample length is the same.
- All data is synchronous, i.e. at the same rate

Channels A,B,C



Item 1	A	Item 2	B	
Item 3	C	Item 4	A	
Item 5	B	Item 6	C	
Item 7	A	Item 8	B	
Item 9	C	Item 10	A	
	⋮			
	⋮			
	⋮			

ODI-2.1 Data Payload- Requirements

IF a device can attain full bandwidth with 8-bit or 16-bit packing
THEN the device **MUST** support 8 and/or 16 bit packing respectively

Required compatibility modes:

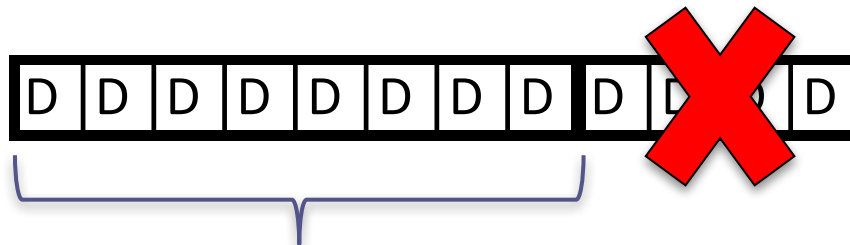
- Concatenate data samples to 8-bit
- Add null data to expand sample to 16-bit
(if sufficient throughput)

IF full resolution of device is >8 bits, but unable to meet throughput requirement with 16-bit packing, THEN the device **MUST** implement link-efficient packing

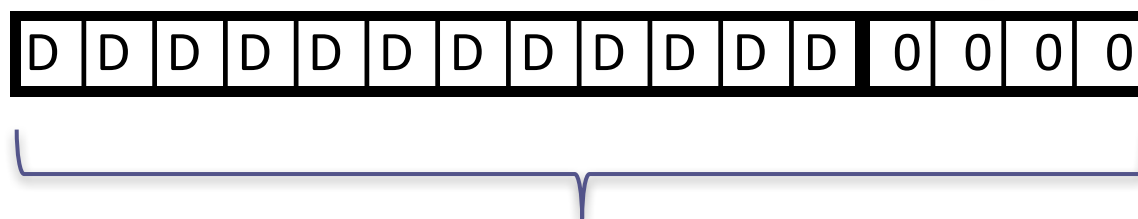


Example: 12-bit data

8-bit packing mode:



16-bit packing mode:

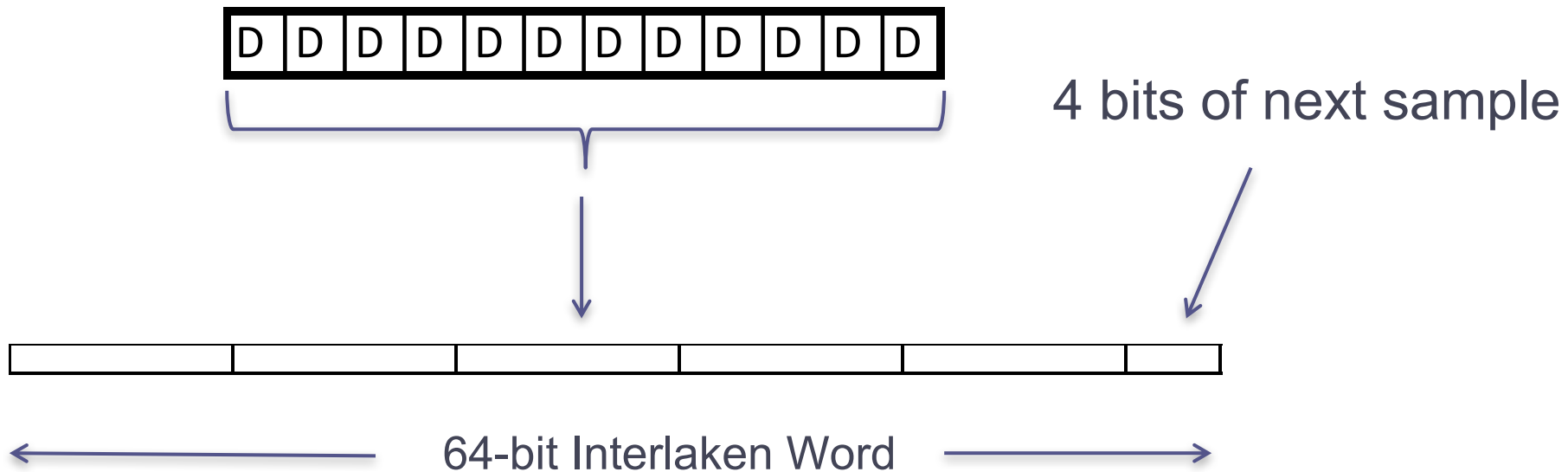


0



Example: 12-bit data, link efficient

Link efficient packing:



ODI-2.1 Data Payload- 32 bytes

- The Data Payload MUST be a multiple of 32 bytes
- Total packet length will then also be a multiple of 32 bytes
- By requiring the packet length to be a multiple of 32 bytes, ODI packets match well with the large electrical bus widths of FPGAs, and reduce the number of possible remainder combinations, the length of the very last electrical bus transfer, to a manageable combination.
- The ODI Technical Committee has reviewed every case of N channels up to 100, B bits from 8 to 16, and packing method. It has determined that for all combinations the producer can choose a sample count per channel per packet that a) is efficient and b) is less than 256KByte packet maximum size, and c) is divisible by 32 bytes.



ODI-2.1 Standardized Context Packet

← 8 Bytes → = 1 Interlaken Word

SOP	
Header	Stream ID
Class ID 1	Class ID 2
TSI	TSF 1
TSF 2	Context Ind.
Bandwidth	
IF Reference Frequency	
RF Reference Frequency	
RF Reference Freq. Offset	
IF Band Offset	
Ref. Level	O-range Cnt.
Sample Rate	
Device Identifier	
EOP	

Context Packets are optional capability that allows a producer to describe metadata about the data stream. ODI-2.1 has developed a standardized Context Packet that is optimized for high-speed RF applications.

ODI-2.1 Context Packet is 96 bytes.

Consists of a 32 byte prologue, followed by 64 bytes of context fields.



Next steps

- Announce ODI set of preliminary specifications to industry at large. Invite participation.
- Finish addressing key technical areas through reviews and interoperability testing.
- Formalize current specifications in textual specification format.
- Address standardized APIs and Test modes, referred to as ODI-A and ODI-T.



Summary

- ODI is abbreviation for Optical Data Interface.
- ODI is an open standard, available to all vendors.
- ODI can attain speeds to 20 GBytes/s per port today, and 80GBytes/s for four ports. Higher speeds in the future.
- ODI addresses 5G, phased array mil/aero, and other high-speed streaming applications difficult with electrical methods.
- ODI works with all instrument formats and all embedded formats through a standardized connector.
- ODI leverages VITA-49 Software Defined Radio packets.
- ODI uses components readily available on the open market.

